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| RF Design Flow –Measurements for Model Generation | |
| HT Micron Semiconductors – Advanced Technology R&D | |
|  |  |
| Classification: | HW TEAM |
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| Revision: | Rev. 0 |
| Date: | 22/08/2020 |
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# Summary

[Summary 2](#_Toc48962269)

[1 DOCUMENT INFO 3](#_Toc48962270)

[2 Test fixture - STANDARD design 3](#_Toc48962271)

[2.1 Proposed Structure 3](#_Toc48962272)

[2.2 Emded/De-Embed Model 3](#_Toc48962273)

[3 Calibration kits design 3](#_Toc48962274)

[3.1 TRL Calibration 3](#_Toc48962275)

[3.2 SOLT Calibration 3](#_Toc48962276)

[4 Test Fixture Design 4](#_Toc48962277)

[4.1 SKYWORKS – SKY66420 4](#_Toc48962278)

[4.2 ST Microelectronics S2-LP die 4](#_Toc48962279)

[4.3 SEMTECH SX1262 die 4](#_Toc48962280)

[4.4 ST Microelectronics BluNRG LP 4](#_Toc48962281)

[5 CONCLUSIONS 4](#_Toc48962282)

[ABBREVIATIONS 5](#_Toc48962283)

[LIST OF FIGURES 6](#_Toc48962284)

[LIST OF TABLES 6](#_Toc48962285)

[REVISION HISTORY 7](#_Toc48962286)

[CONTACT 7](#_Toc48962287)

[DOCUMENT INFORMATION 7](#_Toc48962288)

# DOCUMENT INFO

This document objective is present the SKY66420 RF FEM transmitter path design process. The critical point is design the power amplifier matching network to achieve the transmitter expected performance. The amplifier need work with:

* Operation frequency range: 868MHz to 928MHz
* Constant Gain: 16dB
* Desired output power: 22dBm
* Input Power: 6dBm
* Current consumption around 150mA

The expected current consumption is based on this datasheet curve:

In the future we can optimize the amplifier’s efficiency adjusting the value to a smaller value.

Considering the Gain trade-off for the lower voltage.

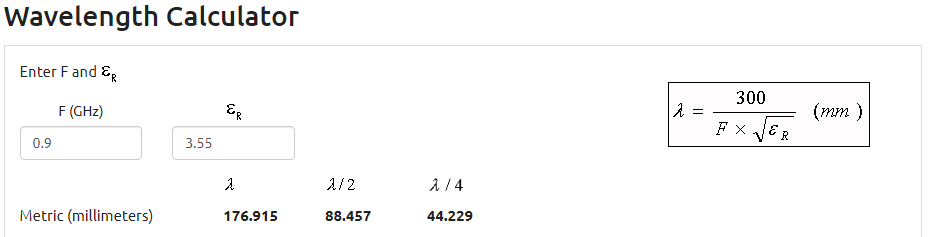
The reference network suggested by the SKYWORKS is implemented in the reference design kit. The schematics is presented here.

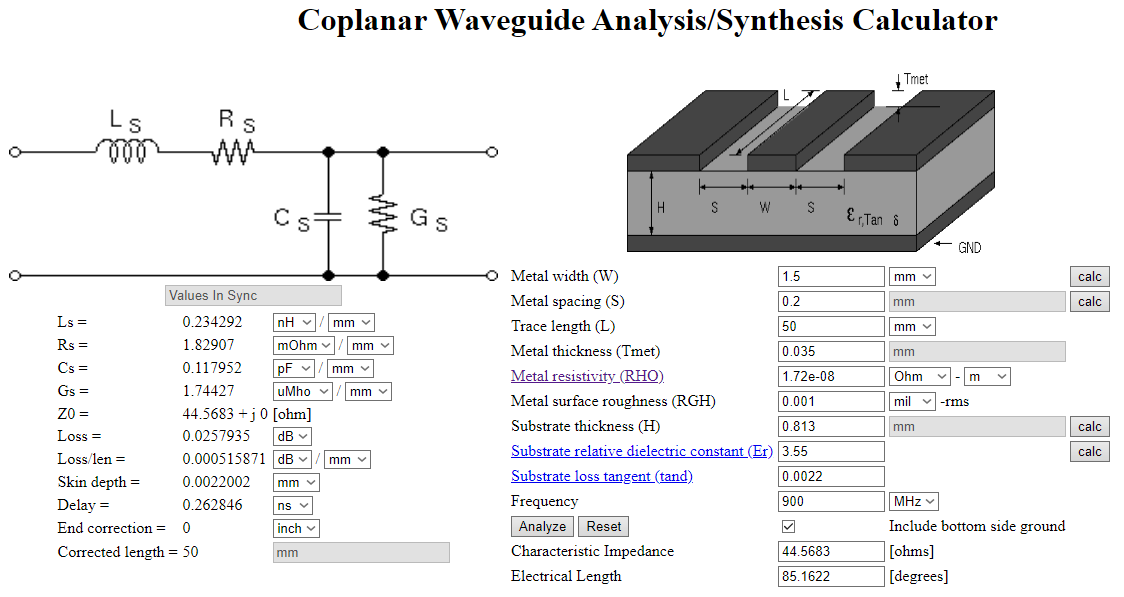
# Test fixture - STANDARD design

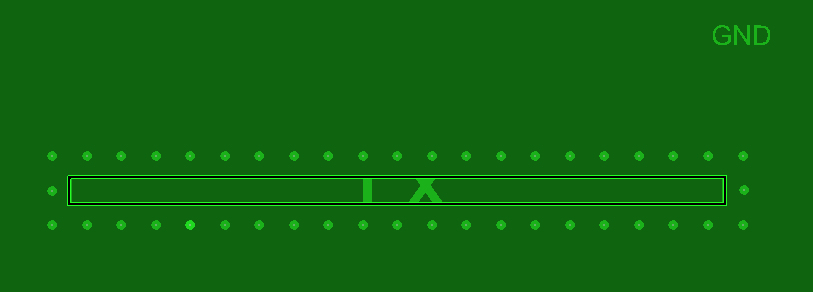
This test fixture is designed to operate in the frequency range of 375MHz to 3GHz. Using the RO4003C laminate with cooper of 35um and core height of 813um.

## Proposed Structure

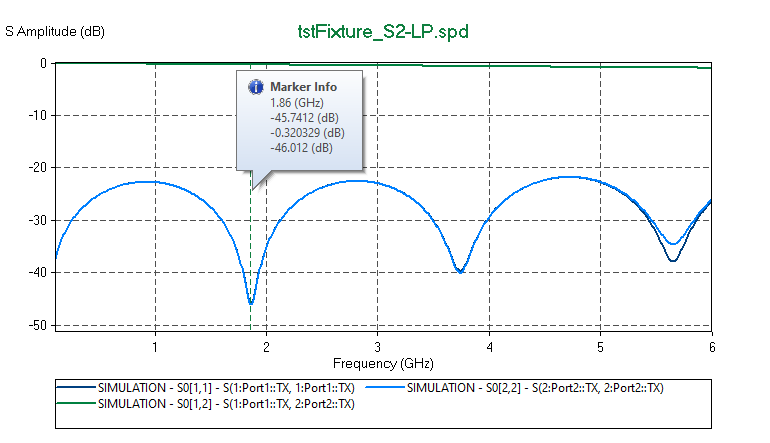
As starting point we use a coplanar waveguide (cpw) calculator (<http://wcalc.sourceforge.net/cgi-bin/coplanar.cgi>) to define the structure parameters and go to an interactive approach into the layout and simulation, where the length of the CPW was estimated considering an wavelength calculator (<https://www.microwaves101.com/calculators/873-wavelength-calculator> ) too.







And the partial results



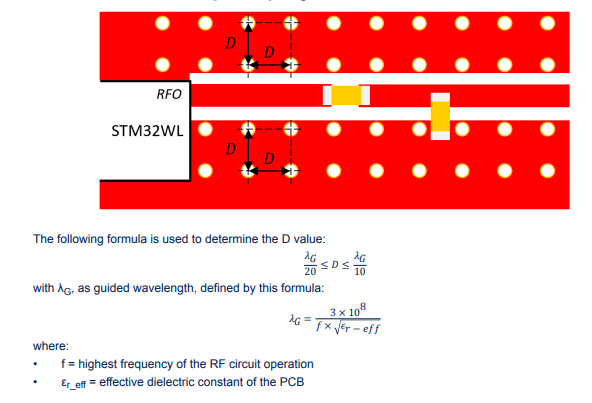
## Test Fixture Design

### Characteristic Impedance Variations

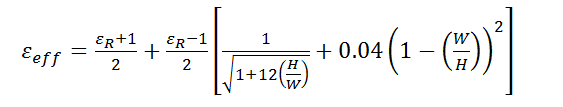
The transmission line width (W=1.65) and the metal spacing (S) varies during the manufacturing process within a 20 % tolerance, then 1.32mm and 1.98mm are expected values for W while 0.16mm and 0.24mm are expected values for S. The length of the transmission line will be affected too: The worst-case analysis shows the following scenarios:

* Higher impedance: W=1.32mm; S=0.24mm
* Lower Impedance: W=1.98mm; S=0.16mm
* Intermediate 1: W=1.98mm, S=0.24mm
* Intermediate 2: W=1.32mm, S=0.16mm

### Via Stitching and shielding



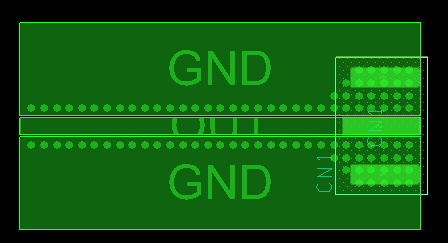
Considering the 9th harmonic from a 3GHz carrier: the higher circuit frequency is 27GHz. Where the effective dielectric constant for W/H<1 is 2.76. (<https://www.pasternack.com/t-calculator-microstrip.aspx> ):

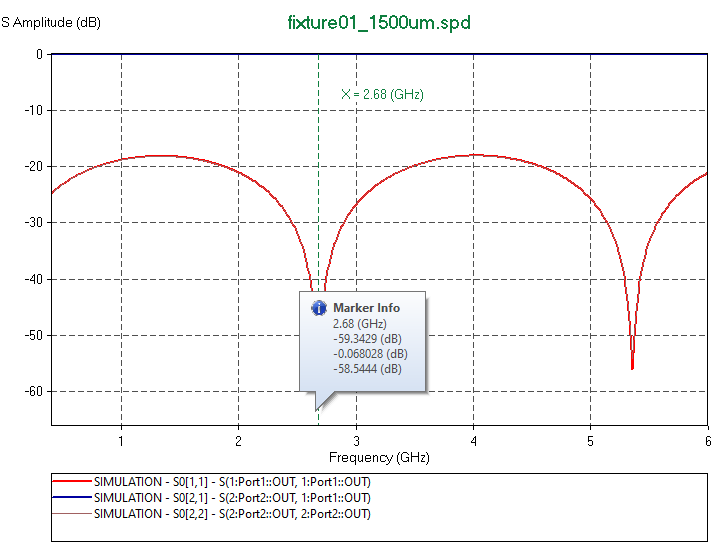


D must be a value between 0.65mm and 1.2mm. We choose spacing of 1.1mm with a cline (from transmission line) offset of 0.8mm.

### Layout and Simulations

The final version has the length of 35mm.





### Worst Case – Process Variations

Note that all the process variations contribute to lower the resonant frequency.

## Emded/De-Embed Model

@ 900MHz

# Calibration kits design

In this approach we will design a new matching network based in four steps:

## TRL Calibration

The choke inductor (L) reactance need to be at least 10 times the value of port impedance, in other words: 80 ohms, the choke inductance value will be:

Doing this, the choke impedance will not be counted in the network design, as long as its minimum value is greater than 15nH. The network was re-designed in the smith-chart, just adjusting the capacitors values:

For this new ideal network,

## SOLT Calibration

Note that the system performance will not be degraded

# Test Fixture Design

## SKYWORKS – SKY66420

## ST Microelectronics S2-LP die

## SEMTECH SX1262 die

## ST Microelectronics BluNRG LP

# CONCLUSIONS

# ABBREVIATIONS

Table 10: Abbreviations

|  |  |
| --- | --- |
| Acronym | Description |
| ADC | Analog to Digital Converter |
| AES | Advanced Encryption Standard |
| API | Application Program Interface |
| CLK | Clock |
| EEPROM | Electrically-Erasable Programmable Read Only Memory |
| FIFO | First in First Out |
| GPIO | General Purpose Input Output |
| ID | Identification |
| IF | Intermediate frequency |
| IO | Input Output |
| MSL | Moisture sensitivity level |
| PCB | Printed-Circuit Board |
| PHY | Physical |
| SPI-bus | Serial Peripheral Interface -bus |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RC | Remote Control |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| RSSI | Receive Signal Strength Indication |
| RX | Receiver |
| SCL | Serial Clock |
| SDA | Serial Data |
| TX | Transmitter |

# LIST OF FIGURES

[Figure 1: Block Diagram 4](#_Toc27131534)

[Figure 2: Pin Diagram 5](#_Toc27131535)

[Figure 3: Package Outline 11](#_Toc27131536)

[Figure 4: Recommended PCB Footprint 12](#_Toc27131537)

[Figure 5: Package Marking Example 12](#_Toc27131538)

# LIST OF TABLES

[Table 1: Pin Description 5](#_Toc27131540)

[Table 2: General Operating Range 8](#_Toc27131541)

[Table 3: Static characteristics: Low-power state power consumption TA = 25 °C, VDD = 3.3 V, 50 MHz crystal oscillator. 8](#_Toc27131542)

[Table 4: Static characteristics: Power consumption in reception TA = 25 °C, VDD = 3.3 V, fc = 905 MHz 8](#_Toc27131543)

[Table 5: Static characteristics: Power consumption in transmission TA = 25 °C, VDD = 3.3 V, fc = 902.2 MHz 8](#_Toc27131544)

[Table 6: Static characteristics: Power consumption in transmission TA = 25 °C, VDD = 3.3 V, fc = 865.2MHz 8](#_Toc27131545)

[Table 7: 50 MHz Internal XTAL clock source characteristics 9](#_Toc27131546)

[Table 8: Transceiver and Receiver characteristics. TA = 25°C based on characterization; not tested in production. VDD = 3.3V; All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%. 10](#_Toc27131547)

[Table 9: Ordering information 13](#_Toc27131548)

[Table 10: Abbreviations 14](#_Toc27131549)

# REVISION HISTORY

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Changes | Authors |
| 01/11/2019 | 00 | - Initial draft | WH |
| 19/11/2019 | 01 | - Initial release | FK |
| 12/12/2019 | 02 | - Review template | SG |
| 29/01/2020 | 03 | - Review styles | WH |

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